

TSMC 98-262  
Serial Number 09/325,951



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### **REMARKS**

Examiner Pompey is to be thanked for careful review of the pending application.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 1, 3-6, and 8-10 remain in this application. Claims 1 and 6 are amended herein. No claims have been allowed. Claims 2 and 7 have been withdrawn

### ***Claim Rejections - 35 U.S.C. § 102***

2. The Examiner has rejected Claims 1-2 and 4 under 35 U.S.C. §102(b) as being anticipated by Liu et al. (U.S. Patent No. 5,739,063, hereinafter Liu et al).

Applicant acknowledges in general the teachings of Liu et al. as cited by the Examiner.

In response, applicant respectfully submits that the key limitation of applicant's invention, which is the formation of a silicon oxide layer on a silicon substrate in an oxidizing environment at least above a minimum temperature, below which temperature are formed deleterious impurity phases within the silicon oxide dielectric layers, is not taught by Liu et al. Therefore, since each and every limitation within applicant's invention as disclosed and claimed within applicant's amended claims 1 and 7 is neither claimed nor disclosed by Liu et al., applicant asserts that

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applicant's amended claim 1 and Claim 4 may not be properly be rejected under 35 U. S. §102 as being anticipated by Liu et al.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of Claims 1-2 and 4 under 35 U.S.C. § 102 as being anticipated by Liu et al. be withdrawn.

***Claim Rejections - 35 U.S.C. §103***

3. The Examiner has rejected Claim 3 and Claims 5-10 under 35 U.S.C. §103(a) as being unpatentable over Higashitani et al. (U.S Patent No. 5,637,528; hereinafter Pong et al.) in view of Wolf (Silicon Processing in the VLSI Era , Vol. 1, pg.209-10, hereinafter Wolf).

Applicant acknowledges in general the teachings of Higashitani et al. in view of Wolf as cited by the Examiner

In response, applicant respectfully submits that the teachings of Higashitani et al. in view of Wolf do not disclose singly or in combination the formation of silicon oxide layers with minimal inclusion therein of impurity phases with deleterious properties as claimed in applicant's amended claim 1 and amended claim 6. Therefore, the citation of Higashitani et al. in view of Wolf over applicant's claims is not properly anticipatory, and may not be properly combined as a basis for rejection of applicant's claim 3, which is dependent upon applicant's amended claim 1. Similarly, the citation of Higashitani et al. in view of Wolf may not properly be combined as a basis for rejection of applicant's claim 5-10. Applicant's Claim 5 is dependent upon applicant's amended claim 1, whose each and

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every limitation is not taught by Higashitani et al. in view of Wolf singly or in combination. Likewise, each and every limitation of applicant's amended Claim 6 and dependent claims 8-10 thereon is not taught by Higashitani et al. in view of Wolf singly or in combination.

In light of the foregoing response, applicant respectfully submits that the Examiners rejection of Claims 3 and 5-10 under 35 U. S. §103 as being unpatentable over Higashitani et al. in view of Wolf et al. be withdrawn.

#### *Discussion*

With respect to the Examiner's citation of the teaching of Liu et al., Higashitani et al. and Wolf, applicant respectfully submits that there is not specifically discussed, disclosed or claimed in any of the aforementioned references employment of an oxidizing method such that formation and annealing of a silicon oxide layer are accomplished with beneficial effects such as control of the rate of oxidation and formation of silicon oxide with desired properties simultaneous with minimization of deleterious formation of impurity species related to out-diffusion of nitrogen species from adjacent silicon nitride layers. The significant limitation of thermally oxidizing to minimize nitrogen out-diffusion, as specified in applicant's amended claims 1 and 6, is therefore not taught by any of the cited references singly or in combination, and therefore may not be properly cited in rejection of applicant's claims to applicant's invention.

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### *Other Considerations*

No fee is due as a result of this amendment.

### **SUMMARY**

Applicant's invention, as claimed within amended Claims 1 and 6 and claims 3-5 and 8-10, is directed toward a method for forming within a silicon semiconductor substrate employed within a microelectronics fabrication a silicon oxide dielectric layer employed as a field oxide (FOX) isolation layer by local dry thermal oxidation of the silicon substrate. In conjunction with applicant's claims 1 and 6 as amended, the prior art of record employed in rejection of applicant's claims to applicant's invention neither claims singly nor in combination each and every limitation within applicants amended claim 1 and amended claim 6, or in the original claims 3-5 and 8-10.

### **CONCLUSION**

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, is respectfully requested.

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Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 914-452-5863 or Mr. George Saile, Esq. (Reg. No. 19,572) at 914-452-5863, at the Examiner's convenience.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'SBA', written over a horizontal line.

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